Brief
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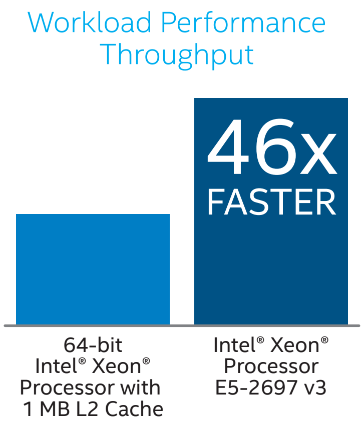
IT@Intel
Increasing EDA Throughput with New Intel® Xeon® Processor E5-2600 v3 Product Family



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Intel's silicon design engineers need significant increases in computing capacity to deliver each new generation of silicon chips. To meet those requirements, Intel IT conducts ongoing performance tests, using the latest Intel silicon design data, to analyze the benefits of introducing compute servers based on new, more powerful processors into our electronic design automation (EDA) computing environment.

We recently tested a dual-socket server based on the latest Intel® Xeon® processor E5-2697 v3, running single-threaded, multi-threaded, and distributed EDA applications operating on more than 500 Intel silicon design workloads. By utilizing all available cores, the server completed workloads up to 46x faster than a server based on a 64-bit Intel® Xeon® processor (3.6 GHz) with a single core. The server was up to 15x faster than a server based on Intel® Xeon® processor 5160 (3.0 GHz) with two cores.

Based on our performance assessment and our refresh cycle, we plan to deploy servers based on the new Intel® Xeon® processor E5-2600 v3 product family this year, completing our replacement of more-than-four-years-old servers based on quad-core Intel® Xeon® processor 5500 series and six-core Intel® Xeon® processor 5600 series. By doing so, we expect to significantly increase EDA throughput while realizing savings, because we can avoid data center construction and reduce power consumption.

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Acronyms

DRC Design Rule Check
EDA electronic design automation
NAC Node Antenna Check
OPC Optical Proximity Correction

Background

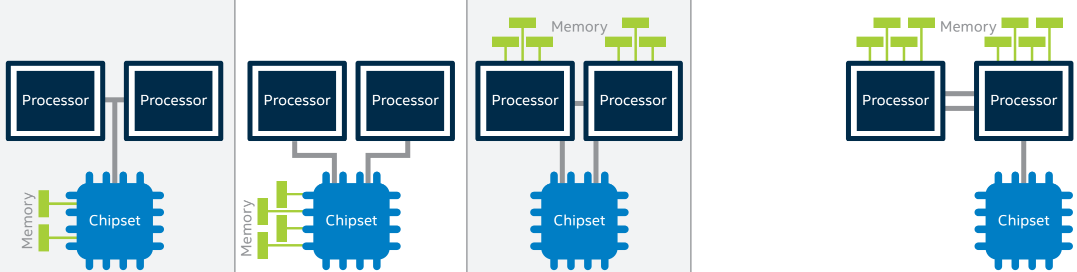
Silicon chip design engineers at Intel face ongoing challenges: integrating more features into ever-shrinking silicon chips, bringing products to market faster, and keeping design engineering and manufacturing costs low.

As design complexity increases, the requirements for compute capacity also increase, so refreshing servers and workstations with higher performing systems is cost-effective and offers a competitive advantage by enabling faster chip design.

Refreshing older servers also enables us to realize data center cost savings. By taking advantage of the performance and power-efficiency improvements in new server generations, we can increase computing capacity within the same data center footprint, avoiding expensive data center construction and achieving operational cost savings due to reduced power consumption.

Intel IT conducts ongoing performance tests, based on the latest Intel silicon design data, to analyze the potential performance and data center benefits of introducing servers based on new processors into our EDA computing environment. Table 1 illustrates some of the architectural enhancements.

Table 1. A Comparison of Dual-Socket Servers Based on Intel® Xeon® Processors



	2004-2005	2006-2008	2009-2011	2012-2014		
Introduction	2004-2005	2006-2008	2009-2011	2012	2013	2014
Intel® Chipset	E7520	5400	5520	C600		C610
Process Technology	90nm	65nm and 45nm	45nm and 32nm	32nm	22nm	
Cores per Socket	1	2 or 4	4 or 6	8	10	14
Cache	1 MB or 2 MB[1]	4 MB or 6 MB shared between 2 cores	8 MB or 12 MB shared	20 MB shared	25 MB shared	35 MB shared
Interconnect Speed	6.4 GB/s	21-25 GB/s	25.6 GB/s per Intel® QuickPath Interconnect	32 GB/s per Intel® QuickPath Interconnect		38.4 GB/s per Intel® QuickPath Interconnect
DIMMs	Up to 8	Up to 16	Up to 18	Up to 24		
Memory Type	DDR2-400 MHz	FB-DIMM/DDR2-667 MHz or FB-DIMM/DDR2-800 MHz	DDR3-800/1066/1333 MHz	DDR3-1333/1600 MHz	DDR3-1333/1600/1866 MHz	DDR4-1600/1866/2133 MHz
Memory Bandwidth	Up to 6.4 GB/s	21-25 GB/s	Up to 32 GB/s	Up to 51.2 GB/s	Up to 59.7 GB/s	Up to 68 GB/s
Maximum Memory	16 GB	64 GB or 128 GB[2]	144 GB or 288 GB[3]	Up to 768 GB[4]	Up to 1536 GB[5]	

[1] Data provided only for 1 MB cache.
[2] 128 GB support with Intel® 5400 Chipset introduced in 2007.
[3] 144 GB assumes 18 memory slots populated with 8-GB DIMMs; 288 GB assumes 18 memory slots populated with 16-GB DIMMs, and validated only with Intel® Xeon® processor 5600 series.
[4] 768 GB assumes 24 memory slots populated with 32-GB DIMMs.
[5] 1536 GB assumes 24 memory slots populated with 64-GB DIMMs.

While our assessments focus on EDA applications, throughput improvements may also be achieved with other applications used in high-performance computing environments where simulation and verification are large parts of the workflow, including:

- Computational fluid dynamics and simulation in the aeronautical and automobile industries
- Synthesis and simulation applications in the life sciences
- Simulation in the oil and gas industries

Test Methodology

We ran tests on dual-socket servers based on Intel Xeon processor E5-2697 v3. This processor includes new features designed to increase throughput compared with previous processor generations, including 22nm process technology, 14 cores, and 35 MB L3 cache.

We ran several tests using industry-leading EDA single-threaded, multi-threaded, and distributed applications comprising more than 500 Intel® Xeon® processor and chipset design workloads.

Our goal was to assess throughput improvement by measuring the time taken to complete a specific number of design workloads. To maximize throughput, we configured each application to utilize all available cores, resulting in one job or process per core. The test configuration is shown in Table 2. We then compared our results with previous tests conducted using the same approach on servers based on the processors.

Maximizing Throughput with Intel® HT Technology

Intel® Xeon® processor E5-2697 v3 with Intel® Hyper-Threading Technology (Intel® HT Technology) can support up to 56 concurrent software threads in a single two-socket platform and deliver higher performance throughput. Intel HT Technology increased performance by up to 1.18x when completing the same number of jobs using 2x the application licenses.

Simulation Jobs Comparison

Time Needed to Complete 113 Jobs on Intel® Xeon® Processor E5-2697 v3

HIGHER IS BETTER

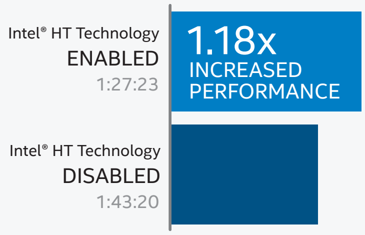


Table 2. Test Configuration for Dual-Socket Servers

	64-bit Intel Xeon® Processor	Intel® Xeon® Processor 5160	Intel® Xeon® Processor X5365	Intel® Xeon® Processor X5460	Intel® Xeon® Processor X5570	Intel® Xeon® Processor X5675	Intel® Xeon® Processor E5-2680	Intel® Xeon® Processor E5-2680 v2	Intel® Xeon® Processor E5-2697 v3
Cores	1	2	4	4	4	6	8	10	14
Frequency	3.6 GHz	3.0 GHz	3.0 GHz	3.16 GHz	2.93 GHz	3.06 GHz	2.7 GHz	2.8 GHz	2.6 GHz
Cache	1 MB	4 MB	8 MB	12 MB	8 MB	12 MB	20 MB	25 MB	35 MB
Interconnect	800 MHz Shared FSB	1333 Dual Independent FSB	1333 Dual Independent FSB	1333 Dual Independent FSB	25.6 GB/s per Intel® QPI link	25.6 GB/s per Intel® QPI link	32.0 GB/s per Intel® QPI link	32.0 GB/s per Intel® QPI link	38.4 GB/s per Intel® QPI link
RAM	16 GB	16 GB	32 GB	32 GB	48 GB	96 GB	128 GB	256 GB	256 GB
Memory Type	DDR2-400 MHz	FB-DIMM/ DDR2-667 MHz	FB-DIMM/ DDR2-667 MHz	FB-DIMM/ DDR2-667 MHz	DDR3-1333[6] MHz	DDR3-1333 MHz	DDR3-1333 MHz	DDR3-1600 MHz	DDR4-2133 MHz[7]

DDR – double data rate; FB-DIMM – fully buffered dual in-line memory module; FSB – front side bus; Intel® QPI – Intel® QuickPath Interconnect

[6] DDR3-1333 RAM running at 1066 MHz.

[7] DDR4-2133 RAM running at 1866 MHz.

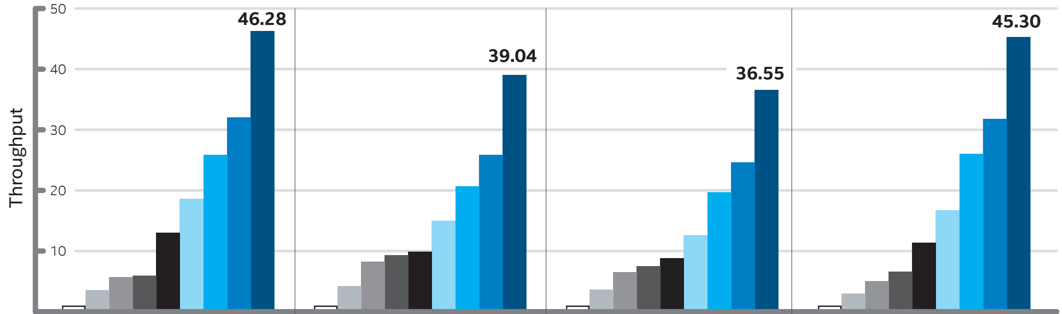
Results

Results are shown in Figure 1; actual runtimes are on the following page in Table 3. The Intel Xeon processor E5-2697 v3-based server completed the tests up to 46x faster than a server based on the single-core 64-bit Intel Xeon processor, and up to 15x faster than a server based on Intel Xeon processor 5160.

46x FASTER

Higher is Better

All cores loaded using 64-bit Intel Xeon processor with 1 MB L2 cache as baseline

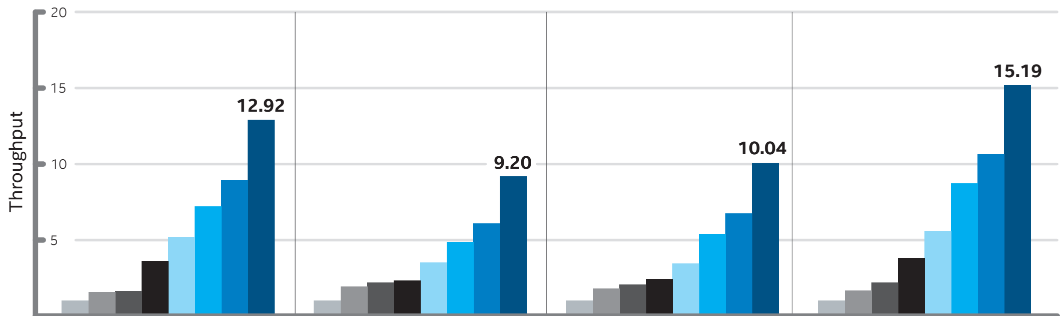


RELATIVE THROUGHPUT	**Simulation** 113 jobs	**Physical Verification** Design Rule Check (DRC) 1,680 jobs	**Physical Verification** Node Antenna Check (NAC) 1,680 jobs	**Optical Proximity Correction (OPC)** 561 templates
Baseline – 64-bit Intel® Xeon® processor	1.00	1.00	1.00	1.00
Intel® Xeon® processor 5160	3.58	4.24	3.64	2.98
Intel® Xeon® processor X5365	5.65	8.22	6.50	5.00
Intel® Xeon® processor X5460	5.91	9.32	7.50	6.60
Intel® Xeon® processor X5570	12.98	9.89	8.84	11.39
Intel® Xeon® processor X5675	18.63	14.98	12.59	16.73
Intel® Xeon® processor E5-2680	25.87	20.70	19.66	25.99
Intel® Xeon® processor E5-2680 v2	32.01	25.86	24.59	31.77
Intel® Xeon® processor E5-2697 v3	**46.28**	**39.04**	**36.55**	**45.30**

15x FASTER

Higher is Better

All cores loaded using Intel Xeon processor 5160 as baseline



RELATIVE THROUGHPUT	**Simulation** 113 jobs	**Physical Verification** Design Rule Check (DRC) 1,680 jobs	**Physical Verification** Node Antenna Check (NAC) 1,680 jobs	**Optical Proximity Correction (OPC)** 561 templates
Baseline – Intel® Xeon® processor 5160	1.00	1.00	1.00	1.00
Intel® Xeon® processor X5365	1.58	1.94	1.79	1.68
Intel® Xeon® processor X5460	1.65	2.20	2.06	2.21
Intel® Xeon® processor X5570	3.63	2.33	2.43	3.82
Intel® Xeon® processor X5675	5.20	3.53	3.46	5.61
Intel® Xeon® processor E5-2680	7.22	4.88	5.40	8.71
Intel® Xeon® processor E5-2680 v2	8.94	6.09	6.75	10.65
Intel® Xeon® processor E5-2697 v3	**12.92**	**9.20**	**10.04**	**15.19**

Figure 1. Electronic Design Automation (EDA) summary test results showing relative throughput of 64-bit Intel® Xeon® processors.
Note: Same application binary used across all the platforms.

Table 3. Electronic Design Automation (EDA) Test Results Showing Runtimes and Workload Configurations

	64-bit Intel® Xeon® Processor with 1 MB L2 Cache	Intel® Xeon® Processor 5160	Intel® Xeon® Processor X5365	Intel® Xeon® Processor X5460	Intel® Xeon® Processor X5570	Intel® Xeon® Processor X5675	Intel® Xeon® Processor E5-2680	Intel® Xeon® Processor E5-2680 v2	Intel® Xeon® Processor E5-2697 v3
SIMULATION (113 CPU MODEL TESTS)									
Number of Simultaneous Jobs	2	4	8	8	8	12	16	20	28
Total Runtime (hh:mm:ss)	79:41:46	22:15:24	14:06:54	13:28:57	6:08:23	4:16:36	3:04:52	2:29:23	1:43:20
Relative Throughput	1.00	3.58	5.65	5.91	12.98	18.63	25.87	32.01	46.28
PHYSICAL VERIFICATION (DESIGN RULE CHECK [DRC])									
Simultaneous 2-Threaded Jobs	1	2	4	4	4	6	8	10	14
Total Number of Iterations	1680	840	420	420	420	280	210	168	120
Total Number of Jobs	1680	1680	1680	1680	1680	1680	1680	1680	1680
Total Runtime (hh:mm:ss)	10918:36:00	2572:58:00	1328:50:00	1171:34:00	1103:40:00	728:46:40	527:27:00	422:08:48	279:42:00
Relative Throughput	1.00	4.24	8.22	9.32	9.89	14.98	20.70	25.86	39.04
PHYSICAL VERIFICATION (NODE ANTENNA CHECK [NAC])									
Simultaneous 2-Threaded Jobs	1	2	4	4	4	6	8	10	14
Total Number of Iterations	1680	840	420	420	420	280	210	168	120
Total Number of Jobs	1680	1680	1680	1680	1680	1680	1680	1680	1680
Total Runtime (hh:mm:ss)	2980:08:00	818:18:00	458:16:00	397:29:00	337:03:00	236:45:20	151:33:00	121:11:36	81:32:00
Relative Throughput	1.00	3.64	6.50	7.50	8.84	12.59	19.66	24.59	36.55
OPTICAL PROXIMITY CORRECTION (OPC) (561 TEMPLATES PROCESSING)									
Number of Simultaneous Jobs	2	4	8	8	8	12	16	20	28
Total Runtime (hh:mm:ss)	10:40:12	3:34:39	2:08:04	1:37:03	0:56:11	0:38:16	0:24:38	0:20:09	0:14:08
Relative Throughput	1.00	2.98	5.00	6.60	11.39	16.73	25.99	31.77	45.30

Conclusion

The new Intel Xeon processor E5-2600 v3 product family delivers significant throughput improvements for Intel design workloads across a range of EDA applications. Using a weighted performance measure of end-to-end EDA applications based on Intel silicon design tests, we found that the effective refresh ratio to replace Intel Xeon processors based on Intel Xeon 5500 series with servers based on the Intel Xeon processor E5-2697 v3 is approximately 4:1.

Based on our performance assessment and our refresh cycle, we plan to deploy servers based on the new Intel Xeon processor E5-2600 v3 product family this year, completing our replacement of older servers based on quad-core Intel Xeon processor 5500 series and six-core Intel Xeon processor 5600 series. By doing so, we expect to achieve greater throughput while realizing operational benefits such as cost avoidance of data center construction and reduced power consumption.

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